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(54) Mounting one integrated circuit upon another

(57) In an integrated circuit assembly a memory chip 3 is mounted on a logic chip 1. A first set of contact pads 2 on the logic chip 1 are electrically joined to corresponding contact pads 4 on the memory chip 3 to secure the chips to one another in face-to-face relationship and to provide interconnections between the chips. A further set of contact pads 5 on the logic chip 1 are provided for external connections to the integrated circuit assembly. The assembly may be contained in a protective package 7, 8 or may be mounted on an etched metal film using a tape assisted bonding technique.

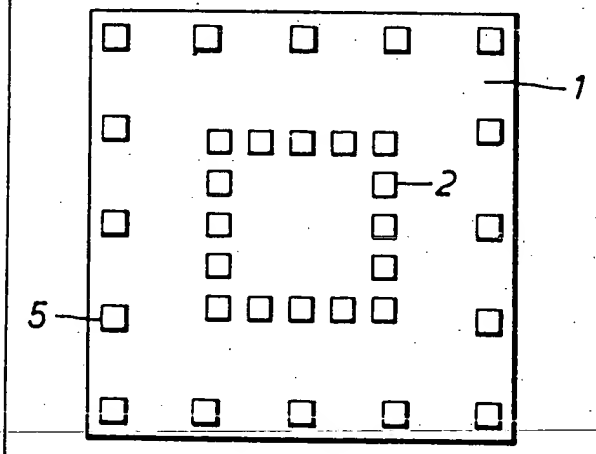

FIG. 2.

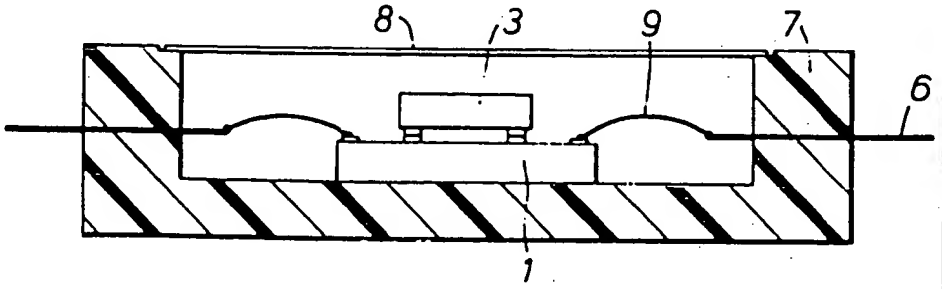

FIG. 3.

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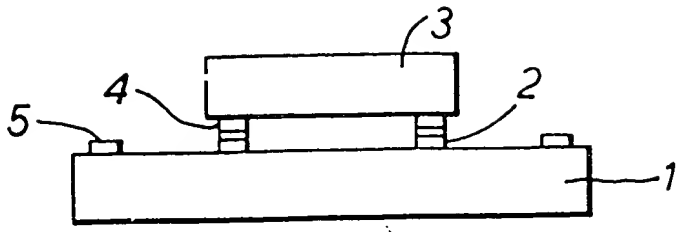

FIG. 1.

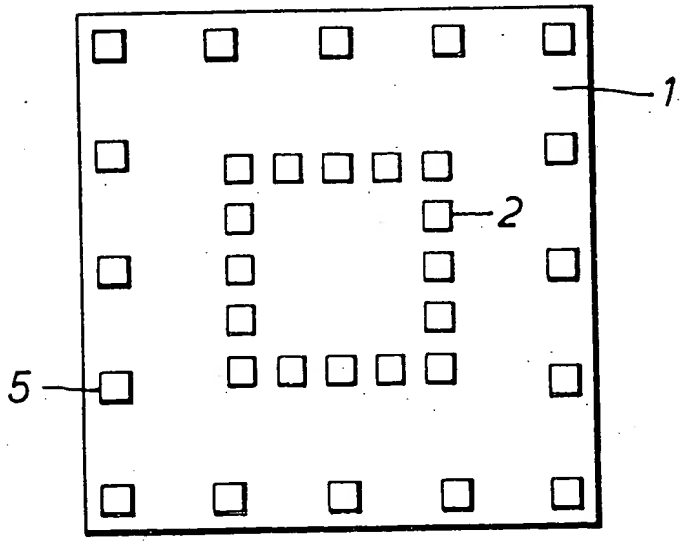

FIG. 2.

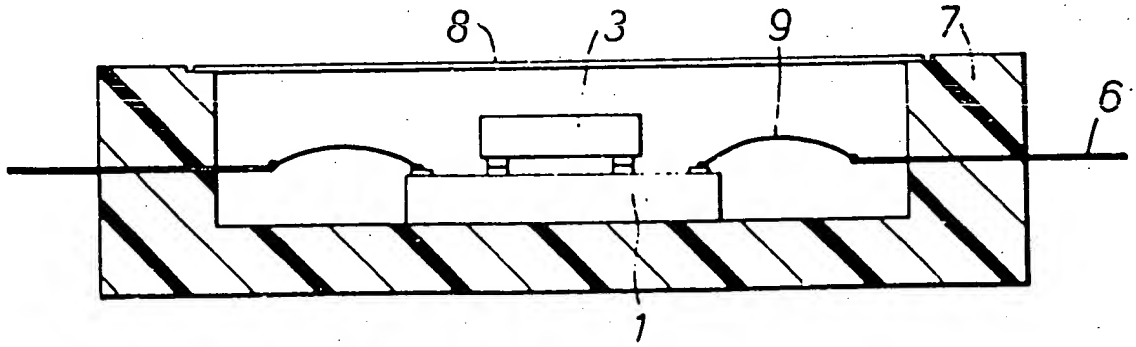

FIG. 3.

SPECIFICATION

Integrated circuit assemblies

The present invention relates to integrated circuit assemblies and in particular to integrated circuit assemblies which include more than one integrated circuit chip.

In the field of data processing it is often required that two or more integrated circuits are functionally linked to one another, for example, an integrated circuit memory may be required to be functionally linked to an integrated circuit providing a logic function.

It has previously been proposed to provide logic and memory functions on a single chip. This arrangement can be provided at a minimum cost and can result in a package which occupies a relatively low area on a printed circuit board, for example. However, such an arrangement provides only one combination of memory and logic functions and thus a different chip is required for every memory or logic variant. The necessity to stock a large number of different chips carrying all memory and logic variations required is a costly operation and hence is a significant disadvantage of this proposal.

It has also been proposed to provide memory and logic functions on separate chips mounted in the same package. This arrangement provides maximum flexibility in that any required combination of memory and logic chip may be included in the package. However, a disadvantage with this arrangement is that contact or bond pads, to which external connections to the chip are made, are required to interconnect the two chips thus reducing the total number of pads available for external connections to the package. Further disadvantages with this arrangement lie in the necessity to provide a substrate to carry interconnections between the two chips and the necessity for an extra assembly operation joining the chips to the interconnections. Also, for example, if the chips are mounted in side by side relationship a larger package which occupies a larger area of a printed circuit board results.

According to the present invention an integrated circuit assembly includes;

a first integrated circuit chip having first and second pluralities of contact pads; and

a second integrated circuit chip having on one face a plurality of contact pads corresponding one with each of the first plurality of contact pads on the first integrated circuit chip when the first and second chips are in face-to-face relationship, the corresponding pairs of contact pads of each chip being bonded to one another to form electrical connections therebetween;

the second plurality of contact pads forming external terminations for the assembly.

Preferably the contact pads on the first integrated circuit chip are on one face thereof, the second plurality of contact pads being positioned around the periphery of the chip and the first plurality of contact pads being positioned within the second plurality.

An integrated circuit assembly will now be described, by way of example, with reference to the accompanying drawing, in which:

Figure 1 is a side view of an integrated circuit memory chip mounted on an integrated circuit logic chip,

Figure 2 is a plan view of the integrated circuit logic chip of Fig. 1, and

Figure 3 shows both integrated circuit chips enclosed in a package.

Referring to the drawings, an integrated circuit logic chip 1 carries a set of contact pads 2 arranged in the form of a square on one of its surfaces. The contact pads 2 are electrically joined to parts of the circuitry of the logic chip 1 which require to be electrically connected to an integrated circuit memory chip 3.

The memory chip 3 has a set of contact pads 4 corresponding in position with the pads 2 on the logic chip 1. The contact pads 4 are electrically joined to parts of the circuitry of the memory chip 3 which are required for electrical connection to the logic chip 1.

The memory chip 3 is mounted on the logic chip 1 in face-to-face relationship as shown in Fig. 1, corresponding pairs of the contacts pads 2 and 4 being electrically joined to one another to complete the required interconnections between the logic and memory chips. The joins also serve to secure the memory chip 3 to the logic chip 1.

The logic chip 1 has a further set of contact pads 5 which are positioned around the periphery of the surface carrying the contact pads 2. The contact pads 5 are electrically joined to those parts of the logic chip circuitry which require to be electrically connected to external terminations 6 of a package 7. The package 7 supports the integrated circuit chips and provides a housing which physically protects the chips. A lid or cover 8 seals the package 7. Conductors 9 electrically connect the contact pads 5 to the external terminations 6 of the package 7.

A method by which the package assembly may be produced will now be described. It will be appreciated that integrated circuit chips normally are provided with a single set of contact pads positioned around the periphery of one of their surfaces. In the case of the logic chip forming part of the present invention an additional set of contact pads are required to be positioned within the boundary of the normal set. A number of logic chips carrying a range of circuit variants may be provided, similarly, a range of memory chips, smaller in size than the logic chips, and with contact pads corresponding to the inner pads

of the logic chip may be provided.

The inner contact pads 2 of the logic chip 1 and the contact pads 4 of the memory chip 3 are each provided with a coating of solder having a convex surface forming so called solder bumps.

After testing, the logic chip 1 is bonded to an inner surface of the package 7 by a conventional low temperature chip attachment process. The memory chip 3, after testing, is positioned in face-to-face relationship with the logic chip 1, the contact pads 2 of the logic chip abutting the contact pads 4 of the memory chip and the solder bumps are caused to reflow by the application of heat. When the solder is allowed to cool and solidify the corresponding pairs of contact pads 2 and 4 are electrically joined securing the memory chip to the logic chip.

The conductors 9 are bonded between the outer set of contact pads 5 on the logic chip and the external terminations 6 of the package 7 by the conventional means such as, for example, a thermocompression or ultrasonic wire bonding technique. Finally, the lid 8 of the package 7 is bonded in place by a conventional bonding technique.

It will be appreciated that the order of assembly described is by way of example only and may, if desired, be varied. For example, the logic and memory chips may be mounted in face-to-face relationship prior to bonding the logic chip to the package.

The structure described has advantages over other structures previously proposed to functionally link integrated circuits in that it provides a choice of different combinations of memory and logic chips, and which occupies little or no extra area on a printed circuit board than a single chip package, hence reducing printed circuit board and assembly costs.

A further advantage is that the electrical load on the memory chip is reduced due to the short interconnections between the chips attained by the face-to-face mounting and this reduced loading improves the operating speed of the device. The face-to-face mounting also minimises parasitic capacitance effects which are sometimes produced in integrated circuit structures.

While an assembly mounted in a package has been described, this idea also applies to an assembly using the TAB (Tape assisted Bonding) technique where chips are mounted on etched metal films. The TAB technique is described in an article entitled "VLSI Packaging" on pages 73 and 74 of "Electronics" December 29, 1981.

While an assembly comprising a memory chip and a logic has been described above, it will be appreciated that both chips may be of the same type, for example, both may be memory chips or both may be logic chips.

CLAIMS

1. An integrated circuit assembly including: a first integrated circuit chip having first and second pluralities of contact pads; and a second integrated circuit chip having on one face a plurality of contact pads corresponding one with each of the first plurality of contact pads on the first integrated circuit chip when the first and second chips are in face-to-face relationship, the corresponding pairs of contact pads of each chip being bonded to one another to form electrical connections therebetween and to secure the chips together; the second plurality of contact pads on the first chip forming terminations for external connections to the assembly.

2. An integrated circuit assembly as claimed in Claim 1, in which the first and second pluralities of contact pads on the first integrated circuit chip are located on one face thereof.

3. An integrated circuit assembly as claimed in Claim 2, in which the second plurality of contact pads are positioned around the periphery of said one face of the chip and the first plurality of contact pads are positioned within the second plurality.

4. An integrated circuit assembly as claimed in Claim 1, 2 or 3 mounted within a common protective package.

5. An integrated circuit assembly as claimed in any preceding claim, in which one of said circuit chips carries memory circuitry and the other of said circuit chips carries logic circuitry.

6. An integrated circuit assembly as claimed in Claim 5, in which said first circuit chip carries the logic circuitry and said second circuit chip carries the memory circuitry.

7. An integrated circuit assembly constructed substantially as hereinbefore described with reference to the accompanying drawing.

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